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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,740	04/12/2007	Johann Helneder	10808/330(In 1344WOUS)	9382

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EXAMINER	
VAN, LUAN V	

ART UNIT	PAPER NUMBER
1795	

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05/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,740	HELNEDER ET AL.	
	Examiner	Art Unit	
	LUAN V. VAN	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-22 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-22 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment of April 24, 2009 does not render the application allowable. Claims 15-22 and 29-33 are pending in the application.

Status of Objections and Rejections

All rejections from the previous office action are withdrawn in view of Applicant's amendment. New grounds of rejection under 35 U.S.C. 103(a) are necessitated by the amendments.

Claim Rejections

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 15, 18-22 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Fanti et al. (US patent 6622907), with further evidence of inherency provided by Kim et al. (US patent 6417089).

Regarding claim 15, Fanti et al. teaches method for electroplating comprising: applying an electrically conductive base layer 16 (Fig. 4) to a substrate 9; applying an auxiliary layer 22 having a better electrical conductivity in comparison with the base layer after applying the base layer; applying a mask layer PR after applying the auxiliary layer; producing a mask with at least one mask opening 23 from the mask layer; patterning the auxiliary layer using the mask (i.e., etching layer 22, column 11 lines 52-

58), wherein the base layer is not patterned or not completely patterned according to the mask (see Fig. 4C); and electroplating at least one layer in the mask opening after the patterning of the auxiliary layer (column 12 lines 8-11).

In addition, Fanti et al. teaches etching the seed layer 22 using a wet chemical etching process (column 9 lines 41-46). Since this is the same etching process as that of the instant invention, the process of Fanti et al. inherently forms an undercut in the seed layer, i.e., auxiliary layer. This inherency is further supported by Kim et al. According to Kim et al., wet etching has an isotropic etching property and therefore causes undercutting of the bump metallurgy under a solder mask (column 1 lines 52-65). Therefore, since wet etching has an isotropic etching property, the seed layer etching process of Fanti et al. would inherently undercut the seed layer under the mask. The undercut would inherently remain after the electroplating process, since the process of Fanti et al. is the same as that of the instant invention.

Regarding claim 18, Fanti et al. teaches applying an insulating layer 14 prior to applying the base layer 16, patterning the insulating layer 14 by producing a contact opening prior to the application of the base layer (Fig. 4A); and applying a part of the base layer 16 in the contact opening (Fig. 4A).

Regarding claim 19, Fanti et al. teaches wherein applying the base layer comprises applying a barrier layer 16 (made of tungsten or titanium-tungsten, column 9 lines 9-12) against copper diffusion, and wherein applying the auxiliary layer comprises applying a layer comprising copper (column 9 lines 22-25).

Regarding claim 20, Fanti et al. teaches electroplating a base layer 28 (i.e., electroplating nickel layer, column 12 lines 13-19); and electroplating a covering layer 26 (i.e., solder bump) after the electroplating of the base layer, and wherein the base layer comprises a different material from the covering layer.

Regarding claim 21, since the base layer, i.e. nickel, and the covering layer, i.e. lead-tin alloy, of Fanti et al. is made of the same material as that of the instant claim, they would inherently have the same melting point properties of the instant claim.

Regarding claim 22, Fanti et al. teaches wherein patterning of the auxiliary layer comprises galvanic patterning (i.e., electrolytic dissolution, column 9 lines 45-46) of the auxiliary layer.

Regarding claim 31, Fanti et al. teaches wherein the galvanic patterning comprises galvanic patterning (i.e., electroetching, column 10 lines 55-61) in the same installation as the electroplating of the layer in the mask opening.

Regarding claim 32, Fanti et al. teaches solders such as SnCuAg, a ternary compound, can be used (column 10 lines 29-32).

Regarding claim 33, Fanti et al. teaches lead-tin alloy (column 10 line 18).

Claims 16, 17, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fanti et al. in view of Shimo et al. (US pub 2003/0102223).

Fanti et al. teaches the method as described above. Fanti et al. differs from the instant claims in that the reference does not explicitly teach whether the second current

density is higher than the initial current density (claim 16), or the specific current density and time duration of the instant claims (claims 17, 29 and 30).

Shimo et al. teach is a method of electroplating copper in a via hole formed on a multilayer substrate comprising the steps of applying a current density of equal to or less than 1.5 ampere per square decimeter to deposit copper film having a thickness of 1 μm or more, and applying a current density on the order of 3 ampere per square decimeter in the second stage (paragraph 22). By performing the electroplating process using a lower initial current, deposition of dendrite crystals is prevented and copper is electrolytically plated densely and uniformly on the surface of the chemical copper plating layer. Also, voids, which affect the reliability, do not occur in the via holes, so that the via holes is plated in a short time (paragraph 36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a low initial current density as taught by Shimo et al. in the method of Fanti et al., because it would prevent the formation of voids in the via holes, and because it would electroplate a dense and uniform layer of metal in the via holes (paragraph 36 of Shimo et al.). Since the electroplating time determines the thickness of the electroplated metal, it would have been obvious to one having ordinary skill in the art to have further modified the electroplating time in order to electroplate metal layers having the desired thickness. While Shimo et al. is directed to method of plating copper in via holes and Fanti et al. is directed to electroplating via holes for forming a solder bump, both are directed to a process of electroplating a metal in via

holes, therefore one having ordinary skill in the art would have a reason with expectation of success from the combination.

Claims 15, 18-22 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fanti et al. in view of Kim et al., assuming that the undercut formation is not inherent.

Regarding claim 15, Fanti et al. teaches method for electroplating comprising: applying an electrically conductive base layer 16 (Fig. 4) to a substrate 9; applying an auxiliary layer 22 having a better electrical conductivity in comparison with the base layer after applying the base layer; applying a mask layer PR after applying the auxiliary layer; producing a mask with at least one mask opening 23 from the mask layer; patterning the auxiliary layer using the mask (i.e., etching layer 22, column 11 lines 52-58), wherein the base layer is not patterned or not completely patterned according to the mask (see Fig. 4C); and electroplating at least one layer in the mask opening after the patterning of the auxiliary layer (column 12 lines 8-11).

Fanti et al. differs from the instant claims in that the reference does not explicitly teach an undercut in the seed layer.

However, it is known in the art that wet etching causes undercutting of an etched layer. According to Kim et al., wet etching has an isotropic etching property and therefore causes undercutting of the bump metallurgy under a solder mask (column 1 lines 52-65).

Therefore, since wet etching has an isotropic etching property, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have expected that the etching process of Fanti et al. would undercut the seed layer under the mask. The undercut would inherently remain after the electroplating process, since the process of Fanti et al. is the same as that of the instant invention.

Regarding claim 18, Fanti et al. teaches applying an insulating layer 14 prior to applying the base layer 16, patterning the insulating layer 14 by producing a contact opening prior to the application of the base layer (Fig. 4A); and applying a part of the base layer 16 in the contact opening (Fig. 4A).

Regarding claim 19, Fanti et al. teaches wherein applying the base layer comprises applying a barrier layer 16 (made of tungsten or titanium-tungsten, column 9 lines 9-12) against copper diffusion, and wherein applying the auxiliary layer comprises applying a layer comprising copper (column 9 lines 22-25).

Regarding claim 20, Fanti et al. teaches electroplating a base layer 28 (i.e., electroplating nickel layer, column 12 lines 13-19); and electroplating a covering layer 26 (i.e., solder bump) after the electroplating of the base layer, and wherein the base layer comprises a different material from the covering layer.

Regarding claim 21, since the base layer, i.e. nickel, and the covering layer, i.e. lead-tin alloy, of Fanti et al. is made of the same material as that of the instant claim, they would inherently have the same melting point properties of the instant claim.

Regarding claim 22, Fanti et al. teaches wherein patterning of the auxiliary layer comprises galvanic patterning (i.e., electrolytic dissolution, column 9 lines 45-46) of the auxiliary layer.

Regarding claim 31, Fanti et al. teaches wherein the galvanic patterning comprises galvanic patterning (i.e., electroetching, column 10 lines 55-61) in the same installation as the electroplating of the layer in the mask opening.

Regarding claim 32, Fanti et al. teaches solders such as SnCuAg, a ternary compound, can be used (column 10 lines 29-32).

Regarding claim 33, Fanti et al. teaches lead-tin alloy (column 10 line 18).

Claims 16, 17, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fanti et al. in view of Kim et al., and further in view of Shimo et al.

Fanti et al. and Kim et al. teach the method as described above. Fanti et al. differs from the instant claims in that the reference does not explicitly teach whether the second current density is higher than the initial current density (claim 16), or the specific current density and time duration of the instant claims (claims 17, 29 and 30).

Shimo et al. teach is a method of electroplating copper in a via hole formed on a multilayer substrate comprising the steps of applying a current density of equal to or less than 1.5 ampere per square decimeter to deposit copper film having a thickness of 1 μm or more, and applying a current density on the order of 3 ampere per square decimeter in the second stage (paragraph 22). By performing the electroplating process using a lower initial current, deposition of dendrite crystals is prevented and copper is

electrolytically plated densely and uniformly on the surface of the chemical copper plating layer. Also, voids, which affect the reliability, do not occur in the via holes, so that the via holes is plated in a short time (paragraph 36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a low initial current density as taught by Shimo et al. in the method of Fanti et al., because it would prevent the formation of voids in the via holes, and because it would electroplate a dense and uniform layer of metal in the via holes (paragraph 36 of Shimo et al.). Since the electroplating time determines the thickness of the electroplated metal, it would have been obvious to one having ordinary skill in the art to have further modified the electroplating time in order to electroplate metal layers having the desired thickness. While Shimo et al. is directed to method of plating copper in via holes and Fanti et al. is directed to electroplating via holes for forming a solder bump, both are directed to a process of electroplating a metal in via holes, therefore one having ordinary skill in the art would have a reason with expectation of success from the combination.

Response to Arguments

Applicants' arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §

706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUAN V. VAN whose telephone number is (571)272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nam X Nguyen/
Supervisory Patent Examiner, Art Unit 1753

LVV
May 8, 2009